CLAIMS:

1. A transistor amplifier circuit having circuitry for cancellation of third order intermodulation distortion (IM3), and circuitry for neutralization of feedback capacitance.

2. The amplifier circuit of claim 1, being a single ended amplifier.

3. The amplifier circuit of claim 1 or 2, the circuitry for feedback capacitance neutralization comprising a current to current feedback transformer and a capacitance parallel coupled at an output path of the amplifier.

4. The amplifier circuit of claim 3, wherein the current to current feedback transformer is also used for setting the input impedance of the amplifier.

5. The amplifier circuit of claim 3 or 4, the current to current feedback transformer comprising a first inductor parallel coupled to an input of the amplifier, and a second inductor series coupled in an output path of the amplifier, the inductors being located to provide inductive mutual coupling.

6. The amplifier of any preceding claim, the circuitry for capacitance neutralization comprising a voltage feedback transformer and a capacitance parallel coupled at an input path of the amplifier.

7. The amplifier circuit of any of claims 3 to 6, further comprising a feedback resistor to compensate for amplifier input resistance.

8. The amplifier circuit of any of claims 2 to 7, an emitter of the transistor being grounded.

9. The amplifier circuit of any of claims 1, or 3 to 8, comprising a differential amplifier having two or more transistors.

10. The amplifier circuit of claim 9, comprising a differential common emitter amplifier.

11. The amplifier circuit of any preceding claim, the circuitry for cancellation of third order intermodulation distortion being located at the input of the amplifier, and being independent of the loading of the transistor due to the neutralization of the feedback capacitance.

12. The amplifier circuit of any preceding claim, the circuitry for cancellation of third order intermodulation distortion comprising resistive out of band terminations.

13. The amplifier circuit of any preceding claim, the circuitry for cancellation of third order intermodulation distortion being arranged such that a termination impedance is given by:

$$R_S(\Delta\omega) \quad (R_S 2\ \omega) = \frac{\beta_F(n+)}{g_m(\ 2n-3\ )}$$

when $C_I - {}_N\ C_d = 2\ g_m$

or

$$Z_{S,}\ (\Delta\omega) \quad \text{[illegible]}\ 2\ \omega) = R_{,C} = \frac{\beta_F(n+)}{2g(\ 2n-3\ )}$$

when $C_I - {}_N\ C_d = 2\ g_m$

where C_{IN} is the total equivalent transistor input capacitance after neutralization of the feedback capacitance.

14. A transistor amplifier circuit arranged in differential or single ended format, and having a first inductor parallel coupled to an input of the amplifier, and a second inductor series coupled in an output path of the amplifier, the inductors being located to provide inductive mutual coupling, and a capacitor parallel coupled to the output path, the capacitor and the inductors being dimensioned to neutralize parasitic feedback capacitance.

15. A transistor amplifier circuit arranged in differential or single ended format, and having a first inductor series coupled to an input of the amplifier, and a second inductor parallel coupled in an output path of the amplifier, the inductors being located to provide

inductive mutual coupling, and a capacitor parallel coupled to an input path, the capacitor and the inductors being dimensioned to neutralize parasitic feedback capacitance.

16. A wireless transceiver having the amplifier circuit of any preceding claim.

17. A method of producing wireless signals using the transceiver of claim 16.

18. An integrated circuit having the amplifier circuit of any of claims 1 to 15.

19. Portable consumer equipment having a wireless transceiver having the amplifier circuit as set out in any of claims 1 to 15.